MC100EPT25

Differential LVECL/ECL to LVTTL Translator

The MC100EPT25 is a Differential LVECL/ECL to LVTTL translator. This device requires +3.3V, –3.3V to –5.2V, and ground. The small outline 8–lead SOIC package and the single gate of the EPT25 make it ideal for applications which require the translation of a clock or data signal.

The VBB output allows the EPT25 to also be used in a single–ended input mode. In this mode the VBB output is tied to the D input for a non–inverting buffer or the $\overline{D}$ input for an inverting buffer. If used, the VBB pin should be bypassed to ground via a 0.01mF capacitator.

- 1.1ns Typical Propagation Delay
- 275MHz Fmax (Clock bit stream, not pseudo–random)
- Differential LVECL/ECL inputs
- Small Outline SOIC Package
- 24mA TTL outputs
- Flow Through Pinouts
- Internal Input Resistors: Pulldown on D, Pulldown and Pullup on $\overline{D}$
- Q Output will default LOW with inputs open or at GND
- ESD Protection: >4000V HBM, >200V MM
- V_{BB} Output
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack. For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 111 devices

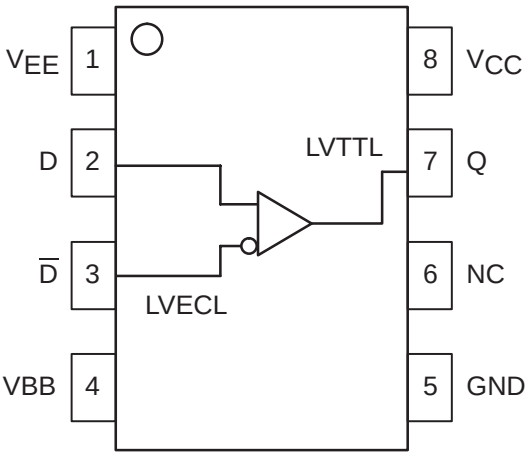

Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

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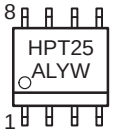
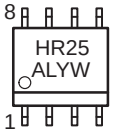
MARKING DIAGRAMS*

SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	**FUNCTION**
Q	LVTTL Output
D, $\overline{D}$	Differential LVECL Input Pair
V_{CC}	Positive Supply
V_{BB}	Output Reference Voltage
GND	Ground
V_{EE}	Negative Supply

ORDERING INFORMATION

Device	Package	Shipping
MC100EPT25D	SO–8	98 Units / Rail
MC100EPT25DR2	SO–8	2500 / Reel
MC100EPT25DT	TSSOP–8	98 Units / Rail
MC100EPT25DTR2	TSSOP–8	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply (Referenced to GND, V_{EE} = –3.3V)	0 to 3.8	VDC
V_{EE}	Power Supply (Referenced to GND, V_{CC} = +3.3V)	–6.0 to 0	VDC
V_I	Input Voltage (V_I not more positive than GND)	0 to 3.8	VDC
I_{out}	Output Current Continuous Surge	50 100	mA
I_{BB}	V_{BB} Sink/Source Current†	± 0.5	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) Still Air 500lfpm	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	41 to 44 ± 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = +3.3V; V_{EE} = –5.5V to –3.0V, GND = 0V)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
IEE	Power Supply Current (Note 1.)	8.0	16	25	8.0	16	25	8.0	16	25	mA
V_{IH}	Input HIGH Voltage Single Ended (Note 4.)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage Single Ended (Note 4.)	–1810		–1625	–1810		–1625	–1810		–1625	mV
V_{BB}	Output Voltage Reference	–1550	–1450	–1350	–1550	–1450	–1350	–1550	–1450	–1350	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			µA

NOTE: 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. (V_{CC} = +3.3V, GND = 0V, V_{EE} = –3.3V), all other pins floating.
2. All loading with 500 ohms to GND, C_L = 20pF.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
4. Input and output parameters vary 1:1 with V_{CC}.

TTL OUTPUT DC CHARACTERISTICS (V_{CC} = 3.3V ± 0.3V; GND = 0V; V_{EE} = –3.3V ± 0.3V; T_A = –40°C to 85°C)

Symbol	Characteristic	Min	Typ	Max	Unit
I_{CCH}	Power Supply Current (Outputs set to HIGH)	6.0	10	14	mA
I_{CCL}	Power Supply Current (Outputs set to LOW)	7.0	12	17	mA
V_{OH}	Output HIGH Voltage (I_{OH} = –3.0mA) (Note 5.)	2.2			V
V_{OL}	Output LOW Voltage (I_{OL} = 24mA) (Note 5.)			0.5	V
I_{OS}	Output Short Circuit Current	–130		–60	mA

NOTE: 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

5. All loading with 500 ohms to GND, CL = 20pF.

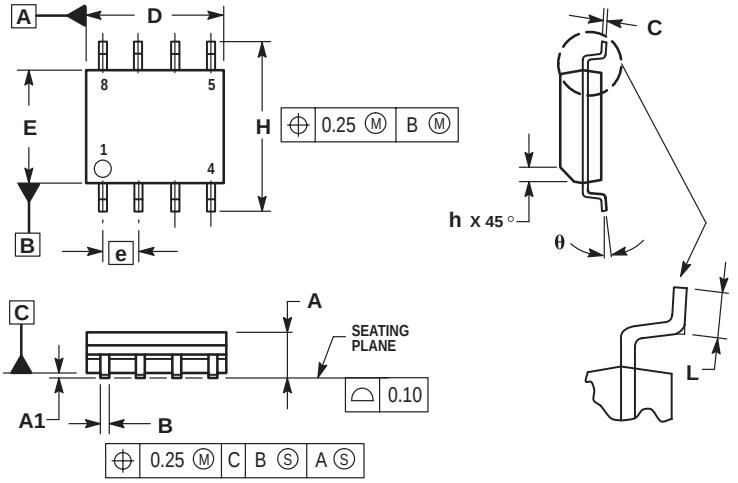
AC CHARACTERISTICS (V_{CC} = 3.3V ± 0.3V; GND = 0V)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency	275			275			275			MHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	800	1200	1800	800	1100	1600	800	1100	1600	ns
t_{SK++} t_{SK--} t_{SKPP}	Output–to–Output Skew++ Output–to–Output Skew– – Part–to–Part Skew (Note 6.)		60 25 500			60 25 500			60 25 500		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Voltage Swing (Differential) (Note 7.)	100	800	1200	100	800	1200	100	800	1200	mV
t_r t_f	Output Rise/Fall Times Q, $\overline{Q}$ (0.8V – 2.0V)	450 900	600 1160	750 1400	450 900	600 1100	750 1400	450 900	600 1100	750 1400	ps

6. Skews are measured between outputs under identical conditions.
7. 200mV input guarantees full logic swing at the output.

PACKAGE DIMENSIONS

SO–8
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751–06
ISSUE T

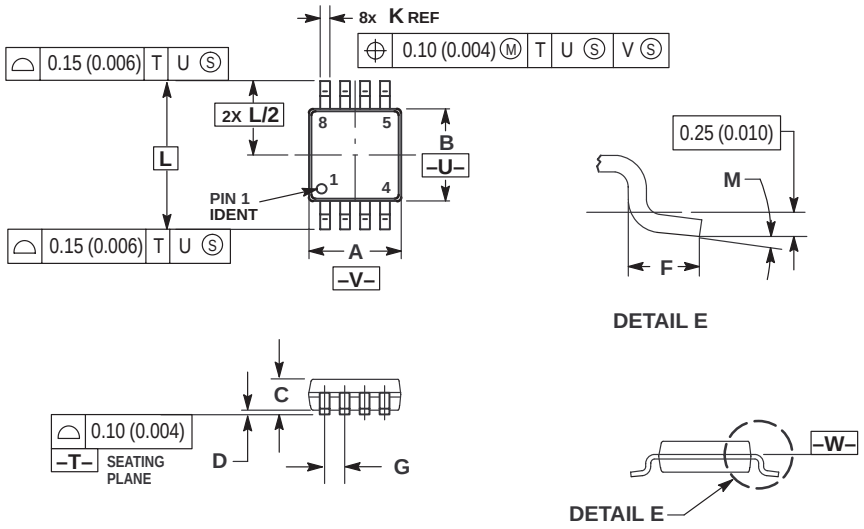


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

PACKAGE DIMENSIONS

TSSOP–8
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948R–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

Notes

Notes

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JAPAN: ON Semiconductor, Japan Customer Focus Center
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